

In the Claims:

Please amend the claims as indicated below.

1. (Currently Amended) An electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages, each of the first and second pipeline stages generating pipeline data;

a latch positioned between the first and second pipeline stages; and

wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal, through the latch; and

wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

2. (Currently Amended) The An electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit configured being adapted to provide the enable signal to the latch to control the latch with the enable signal when the electronic circuit is in the normal mode, and configured to hold the latch open by preventing the enable signal from being provided to the latch when the electronic circuit is in the reduced mode.

3. (Currently Amended) The An electronic circuit as claimed in claim 2, wherein the latch control circuit receives the control signal indicating whether the mode of operation of the electronic circuit operates in the normal mode or in the reduced mode.

4. (Currently Amended) The An electronic circuit as claimed in claim 1, wherein the electronic circuit is adapted to process a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage.

5. (Currently Amended) The An electronic circuit as claimed in 4, wherein the electronic circuit is adapted to operate in the normal mode until an instruction of the third type of instruction is processed.

6. (Currently Amended) The An electronic circuit as claimed in claim 5, wherein, after the instruction of the third type of instruction is processed, the electronic circuit is adapted to operate in the reduced mode if the an instruction, following the instruction of the third type of instruction, is of the second type of instruction or the third type of instruction.

7. (Currently Amended) The An electronic circuit as claimed in claim 4, wherein the electronic circuit is adapted to operate in the reduced mode until an instruction of the first type of instruction is processed.

8. (Currently Amended) The An electronic circuit as claimed in claim 1, wherein the first type of instruction includes a load instruction, and wherein the first and second pipeline stages are asynchronous pipeline stages that are each controlled responsive to different enable signals.

9. (Currently Amended) The An electronic circuit as claimed in claim 1, wherein the second type of instruction includes an arithmetic computation instruction.

10. (Currently Amended) The An electronic circuit as claimed in claim 4, wherein the third type of instruction includes compare, store, branch and jump instructions.

11. (Currently Amended) The An electronic circuit as claimed in claim 1,
wherein the first pipeline stage comprises a data memory.

12. (Currently Amended) The An electronic circuit as claimed in any claim 1,
wherein the second pipeline stage comprises a write back stage.

13. (Currently Amended) A method of operating an electronic circuit, the
electronic circuit being adapted to process a plurality of types of instruction, the
electronic circuit comprising first and second pipeline stages and a latch positioned
between the first and second pipeline stages, the method comprising:

controlling modes of the electronic circuit in response to a control signal that is
based on a latency period of each respective instruction of said plurality of types of
instruction, said electronic circuit being in a normal mode when processing a first type of
instruction in which the latch is opened and closed in response to an enable signal, and a
reduced mode including a truncated passage when processing a second type of instruction
in which the enable signal is overridden by the control signal so that the latch is held
open for the second type of instruction to propagate, independent of the enable signal,
through the latch; wherein the first type of instruction requires processing by the first and
second pipeline stages and the second type of instruction requires processing by the
second pipeline stage.

14. (Currently Amended) The [[A]] method as claimed in claim 13, wherein ~~the~~
~~step of~~ controlling the electronic circuit further includes processing a third type of
instruction, wherein the third type of instruction does not require processing by the
second pipeline stage.

15. (Currently Amended) The [[A]] method as claimed in claim 14, further
comprising ~~the step of~~ operating the electronic circuit in the normal mode until an
instruction of the third type of instruction is processed.

16. (Currently Amended) The [[A]] method as claimed in claim 15, wherein, after processing the instruction of the third type of instruction, the method further comprises the step of operating the electronic circuit in the reduced mode if the an instruction, following the instruction of the third type of instruction, is of the second type of instruction or the third type of instruction.

17. (Currently Amended) The [[A]] method as claimed in claim 14, further comprising the step of operating the electronic circuit in the reduced mode until an instruction of the first type of instruction is processed.

18. (Currently Amended) The [[A]] method as claimed in claim 13, wherein the first type of instruction includes a load instruction, and wherein the enable signal is provided to the latch in the normal mode to open and close the latch, and the control signal prevents the enable signal from being provided to the latch in the reduced mode.

19. (Currently Amended) The [[A]] method as claimed in claim 13, wherein the second type of instruction includes an arithmetic computation instruction, and wherein the first and second pipeline stages are asynchronous pipeline stages that are each controlled responsive to different enable signals.

20. (Currently Amended) The [[A]] method as claimed in claim 14, wherein the third type of instruction includes compare, store, branch and jump instructions.